REMARKS

Reconsideration and allowance of the subject application in view of the foregoing amendments and the following remarks is respectfully requested.

Claims 1-24 are pending.

Claims 1-24 are patentable over *Klein et al.* (US 6,145,102) in view of *Garnett et al.* (US 7,124,321)

The rejection of claims 1-24 under 35 USC 103(a) as being unpatentable over *Klein* in view of *Garnett* is hereby traversed. There are at least three reasons claim 1 is patentable over *Klein* and withdrawal of the rejection is respectfully requested.

The PTO admits that *Klein* does not teach reading, from at least one CPU register, a CPU maximum power value indicating the maximum power the CPU is rated to consume during operation.

First, *Klein* fails to disclose invoking a first error handler "if the CPU maximum power value exceeds the host maximum power value" as claimed in claim 1. That is, *Klein* appears to describe monitoring of the current/voltage of the power supply without specifying whether the monitored current/voltage is that which is received by the power supply or that which is being drawn from the power supply. The PTO-identified portion of *Klein*, reproduced herein for ease of reference, states:

> Also, for example, power supply monitor 134 <u>monitors power supply voltages,</u> and is coupled to interface 135. Interface 135 is coupled to management bus 120. The <u>actual voltage and current on each power supply circuit can be monitored</u> and reported to the system manager 502 by transmission of a message over the network. Alternatively, power supply monitor 134 can have limits set therein, and a message is transmitted to the system manager 502 in the event that a voltage or current exceeds the set limits.

> *Klein* at column 3, line 64 through column 4, line 5.

The PTO-identified portion of *Klein* appears to describe monitoring of the power supply

circuit **without** describing determining if a CPU maximum power value exceeds a host maximum power value. *Klein* recites that the "actual voltage and current on each power supply circuit [is] monitored." Thus, *Klein* fails to disclose or suggest invoking a first error handler if a CPU maximum power value exceeds a host maximum power value. For at least this reason, withdrawal of the rejection is respectfully requested.

Second, *Garnett* fails to disclose "reading from at least one CPU register, a CPU maximum power value" as claimed in claim 1. *Garnett* appears to describe an environment monitor ENV MON 295 storing a limit value in a limit register, however, ENV MON is not a CPU register nor does *Garnett* appear to describe or depict the environment monitor as a CPU register. FIG. 12 depicts ENV MON as a component of switch 73 and not part of processor 240 or even processor 301 of SSP 74. Neither of processor 240 or processor 301 appear to be described as including a register storing a CPU maximum power value. For at least this reason, withdrawal of the rejection is respectfully requested.

Third, the PTO has failed to articulate a rationale or identify a teaching, suggestion, or motivation for combining the applied references. The PTO asserts that a person of ordinary skill in the art at the time of the present invention would have been motivated to combine *Garnett* with *Klein* because "the registers allow for comparisons to be made of the limit values." The PTO appears to be relying on Applicant's claimed subject matter as a road map for combining the pieces of the applied references.

Further, the PTO's purported reason for combining fails to set forth a reason to combine the references, rather the reason stated sets forth an end result based on the present claimed subject matter. That is, the PTO has set forth what is asserted to be a result of combining the references instead of articulating a reasoned basis for why a person of ordinary skill in the art at the time of the present invention would have combined the references. For at least this reason, withdrawal of the rejection is respectfully requested.

Further still, because *Garnett* fails to describe a CPU register storing a CPU maximum power value, *Garnett* fails to disclose subject matter curing the noted deficiency of *Klein*. Applicants fail to understand why a person of ordinary skill in the art would have combined

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Garnett with *Klein.*

Based on each of the foregoing reasons, claim 1 is patentable over *Klein*, singly or in combination with *Garnett*, and withdrawal of the rejection of claim 1 is respectfully requested.

Claims 2-12 depend, either directly or indirectly, from claim 1, include further limitations, and are patentable over *Klein* in view of *Garnett* for at least the reasons advanced above with respect to claim 1. The rejection of claims 2-12 should be withdrawn.

Claim 13 is patentable over *Klein* in view of *Garnett* for at least reasons similar to those advanced above with respect to claim 1 and withdrawal of the rejection of claim 13 is respectfully requested.

Claims 14-24 depend, either directly or indirectly, from claim 13, include further limitations, and are patentable over *Klein* in view of *Garnett* for at least the reasons advanced above with respect to claim 13. The rejection of claims 14-24 should be withdrawn.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that the present application should be in condition for allowance and a Notice to that effect is earnestly solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

Paul BROYLES

Randy A. Noranbrock
Registration No. 42,940
Telephone: (703) 684-1111

HEWLETT-PACKARD COMPANY
IP Administration
Legal Department, M/S 35
P.O. Box 272400
Fort Collins, CO 80528-9599
Telephone: (970) 898-7057
Facsimile: 281-926-7212
Date: **August 7, 2007**
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